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.synopsys\_dc.setup Synopsys Design Compiler Setup File, Which Defines Search Paths, Library Name, Etc. Constraints.tcl The Constraints That Are Used In The Synthesis Lab. Dft.tcl Reference Script In This Lab 1th, 2024

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3. Write The Verilog Program For Your Design (e.g.: Codefile1.v) Gedit Codefile1.v 4. Write The Verilog Test Bench Program For Your Design (e.g.: Codefile1\_tb.v). Now, The Design Entry Using HDL Gets Finished. Gedit Codefile1\_tb.v II. STEPS FOR SIMULATION: 1. Initially, Both Of Your Verilog Programs Have To Be Compiled 2. 3th, 2024

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