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Simulate An 8-bit Ripple-carry Adder Using The 4-bit Adders From Lab 1. The 4-bit Ripple-carry Adder From Lab 1 (VHDL Version) Will Be Used As A Component In This Design. Use PORT MAP Statements To Specify The 8-bit Adder. Modify The Provided Testbench (adder_tb From Lab 1) And Perform A Timing Simulation. Jul 3th, 2024.

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