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Chapter 8 Memory Hierarchy And Cache Memory

• Suppose Processor Has 2 Levels Of Hierarchy: Cache

And Main Memory • T Cache = 1 Cycle, T MM = 100 Cycles • What Is The AMAT Of The Program From Example 1? AMAT = T Cache + MR Cache (t MM) = [1 + 0.375(100)] Cycles = 38.5 Cycles Memory Performance Example 2 3th, 2024

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Only 1 Layer (contact Mask) Is Used To Program Memory Array Programming Of The Memory Can Be Delayed To One Of Last Process Steps ROM Layout Precharged ROM WL[0] WL[1] WL[2] WL[3] BL[0] BL[1] BL[2] BL[3] GND GND VDD Precharge Devices φ pre PMOS Precharge Device Can Be Made As Large 3th, 2024

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A Matter Of Time And Sophiatown Would Be Reborn" (Mattera, 2009, P. 152). Mattera Would Probably Be The First To Admit That Memory Does Not Offer Complete Salvation. In A Seemingly Discordant And Hanging Last Sentence Of The Book – A Sente 3th, 2024

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The Memory/Storage Hierarchy And Virtual Memory

Storage Device Speed Vs. Size Facts: •CPU Needs Subnanosecond Access To Data To Run Instructions At Full Speed •Faststorage (sub-nanosecond) Is Small (100-1000 Bytes) •Big Storage (gigabytes) Is Slow (15 Nanoseconds) •Hugestorage (terabytes) Is Glaciallyslow (milliseconds) Goal: •Need Many Gigabytes Of Memory 2th, 2024

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Storage Involves Maintaining The Information Available In Memory - Whenever People Have Access To Information They No Longer Sense, Memory Is Involved 15 It's A Memory When... Example- If You Look Up A Phone Number, Go To The Telephone, And Dial The Number Then Memory Is Involved- Even If For Only Second 3th, 2024

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Secondary Memory Memory Hierarchy

Secondary Memory Memory Hierarchy: In Modern

Computers, There Are Several Types Of Memory: • Cache: RAM Technology Capacity 256K- 1 M, 10 Nanoseconds • Main Memory: RAM - ROM Technology 100 M- 1G, 100 Nanoseconds • Secondary Storage (Disk): 10 G-1000 G, 10-30 Milliseconds • Tert 2th, 2024

Cache Memory And Performance Memory Hierarchy 1

Memory Hierarchy 19 CS@VT Computer Organization II © 2005-2015 CS:APP & McQuain Caches Cache: A Smaller, Faster Storage Device That Acts As A Staging Area For A Subset Of The Data In A Larger, Slower Device. Fundamental Idea Of A Memory Hierarchy: – For Each K, The Faster, Smaller Device At Level K Serv 2th, 2024

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