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Featuring A Single Core And 512 MByte Of DRAM With  
A 1GHz Processor. MicroSoM I1 Highlighted Features: •  
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To Be Used With Certified Power Adaptor With Output  
Rated 5VDC, 3A. Power Adapter Must Meet Limited  
Power Source (LPS) Requirements Mar 3th, 2024

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Overview . At Only 2 ×2 ×2 The CuBox -i Is The Tiniest  
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### **Freescale I.MX6 DRAM Port Application Guide- DDR3**

Data Bus/DQM And DQS Of Each Byte Must Be Matched  
In Upper And Lower Byte Connection. For Example,  
D0-D7, DQM0, DQS0/DQS0\_B... D56-D63, DQM7,  
DQS7/DQS7\_B Should Be In Same Byte Connection.  
Layout Checking List 1 100Ω Differential Impedance  
Control (DQS And CLK Signals) And 50Ω Impedance  
Con Jan 3th, 2024

### **NXP I.MX6 Cortex-A9**

WANDBOARD ORG Dimensional Drawing NXP I.MX6  
Cortex-A9 Low Cost Open Source Community  
Development Board Block Diagram Jan 3th, 2024

### **MX6 10.6eV PID Response Factor Table**

Sep 21, 2018 · Methyl Benzyl Alcohol STYRENE  
ALCOHOL 13323-81-4 C8H10O 0.80 Methyl T-butyl  
Ether MTBE, Tert-Butyl Methyl Ether 1634-04-4

C5H12O 9.24 40 0.86 MEK (Methyl Ethyl Ketone)  
2-Butanone 78-93-3 C4H8O 9.51 200 0.90 Methyl  
Isobutyl Ketone MIBK, 4- Feb 1th, 2024

### **MIPI-CSI2 Peripheral On I.MX6 MPUs**

For More Details, See Section 2.3.1 “Bandwidth”. The I2C Bus Is Required To Configure Most Of The Camera Sensors. 2.1. Routing MIPI Stream Into CSI-2 The I.MX6 Processors Have One MIPI/CSI-2 Input And Two Parallel Input Interfaces (parallel 0 And Parallel 1; See Figure 2). The Streams In The MIPI Format Apr 1th, 2024

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