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(the More Common 4-wire Serial Interface Used To Connect Serial Peripheral Interfaces To A Microprocessor Or Host). The Design Uses The MAX II CPLD To Bridge An SPI Host To Communicate With Devices Connected On An I2S Bus. In Figure 1, The MAX II CPLD Bridge Is Seen As An SPI Slave To The SPI May 2th, 2024

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AOC-MTGN-i2S

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