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Enabling SPI-based Flash Memory Expansion By Using ...Memory Via Serial Peripheral Interface (SPI) Protocol, Routed By A Multiplexer (mux). Figure 1 Shows How A Mux Routes The SPI Signal To Give Users Multiple Ways To Access The Flash Memory, Either Through The FPGA Or An External Header. The Header Allows External Access To The Flash Me 3th, 2024SPI (Serial Peripheral Interface) NAND Flash MemorySPI NAND Flash Supports Quad SPI Operation When Using The X4 And Quad IO Commands. These Commands Allow Data To Be Transferred To Or From The Device At Four Times The Rate Of The Standard SPI. When Using The Quad SPI Command The SI And SO Pins Become Bidirectional I/O Pins: SIOO A 4th, 20243V 128M-BIT SERIAL FLASH MEMORY WITH DUAL/QUAD SPI ...- Quad SPI: CLK, /CS, IO 0, IO 1, IO 2, IO 3 - QPI: CLK, /CS, IO 0, IO 1, IO 2, IO 3 - Software & Hardware Reset Highest Performance Serial Flash - 104MHz Single, Dual/Quad SPI Clocks - 208/416MHz Equivalent Dual/Quad SPI - 50MB/S Continuous Data Transfer Rate - - More Than 100,000 Erase/program Cycles 3th, 2024.

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