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EECE488 Analog CMOS Integrated Circuit Design Assignment 4 Due: Tuesday November 26th, 2013 At 8:00am 1. Consider

The Following Circuit. (This Circuit Is Sometimes Referred To As A Self-biased Current Source). $R = V_{DD} - V_{TH}$, $V_{DD} = 3V$, $V_{TH}(NMOS) = 0.3V$, $V_{TH}(PMOS) = 0.4V$. Assume All Transistors Are Operating In Saturation Region And $\beta_n = 4\beta_p$. $V_{DD} = 3V$, $V_{TH}(NMOS) = 0.3V$, $V_{TH}(PMOS) = 0.4V$. 3th, 2024

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