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05-01-2011 Chirag Sangani References •R. Haskell, D. Hanna: "Introduction To Digital Design Using Digilent FPGA 1th, 2024

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Into One Circuit With One Common Binary Adder. This Is Done By Including An Exclusive-OR Gate With Each Full Adder. A 4-bit Adder-subtractor Circuit Is Shown In Figure 2. Input S Controls The Operation. 1. When S = 0 The Circuit Is An Adder. 2.

When S = 1 The Circuit Becomes A Subtractor. 3th, 2024

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Prototype The Nuclei Evaluation SoC (included RISC-V Core) In FPGA Boards; And The Nuclei Made JTAG Debugger Kit (called Hummingbird Debugger Kit), Which Can Be Used To Debug The RISC-V Core In FPGA Prototype Or In Real Chip. Figure 1-1 3th, 2024

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Digilent's PC-based Program Called Adept Can Be Used To Configure The FPGA With Any Suitable Bit File Stored On The Computer. Adept Uses The USB Cable To Transfer A Selected Bit File From The PC To The FPGA (via The FPGA's JTAG Programming Port). Adept Can Also Program A Bit File I 3th, 2024

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