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CMOS Image Sensor Technology Achieves The Full Frame Rate In ... Work Was Supported By The Knowledge Cluster Initiative Of Ministry Of Educa- ... Demonstrated In Many Developments [5]-[7]. The ...
Jan 1th, 2024

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Denote This Maximum Difference By Δ , With The Understanding That The Overall Lock Range Is In Fact Around Δ . The Dependence Of The Lock Range Upon The Injection Level, I_{inj} , Is To Be Expected: If I_{inj} Decreases, Δ Must Form A Greater Angle With So As To Maintain The Phase Difference Between And At [Fig. 3(d)]. Thus, The Circuit Moves Closer To Jan 1th, 2024

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 4 ...

Analyses Of Injection-locked Oscillator Are Only Applicable To LC Oscillators [15]–[18], We Propose New Analytical Equations That Enable The Understanding Of Injection-locked, Nonharmonic Ring Oscillators, Including The Locking Range, Phase Deskew Ability, And Jitter Performance. Details Of The Receiver Circuit Jan 2th, 2024

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Analog-to-Digital Converter Heemin Y. Yang And Rahul Sarpeshkar, Member, IEEE Abstract—Dual-slope Converters Use Time To Perform Analog-to-digital Conversion But Require $2 + 1$ Clock Cycles To Achieve Bits Of Precision. We Describe A Novel Current-mode Algorithm That Also Uses Time To Perform Analog Feb 3th, 2024

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Ated With Respect To (gate Width Of) And (gate Width Of), Respectively. It Results In Two Conditions To Satisfy, I.e., (a) And (b) . Also, The Condi-tion Of Reduces The Noise Con-tribution From Significantly, As Described In Appendix III. In This Work, The Gate Widths Of And Are Chosen To Be 60 And 120 M, R May 3th, 2024

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To Reduced Integrator Gain At High Frequency. Another Work Proposed To Place The VCO Quantizer At

The Latter Stage Of A Sub-ranging Architecture To Minimize Its Input [13] [Fig. 1(c)]. But The Overall Performance Was Limited By The Digital-to-analog Converter (Mar 1th, 2024

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450 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 2, FEBRUARY 2009 Systematic Transistor And Inductor Modeling For Millimeter-Wave Design ChuanKang Liang, Student Member, IEEE, And Behzad Razavi, Fellow, IEEE Abstract—This Paper Proposes A Simulation-based Modeling Methodology That Provides Greater flexibility In The Design And Apr 3th, 2024

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Payam Heydari, Senior Member, IEEE Abstract—Integration Of Multi-mode Multi-band Transceivers On A Single Chip Will Enable Low-cost Millimeter-wave Systems For Next-generation Automotive Radar Sensors. The first Dual-band Millimeter-wave Transceiver Operating In The 22–29-GHz And 77–81 Jan 2th, 2024

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DB SNDR At Nyquist Rate Sedigeh Hashemi And Behzad Razavi, Fellow, IEEE Abstract—A Two-stage Pipelined ADC Employs A Double-sam- Pling Jul 3th, 2024

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Higher SNDR. The Modulator Achieves 82-dB Dynamic Range And 81-dB Peak SNDR In The A-weighted Audio Signal Bandwidth With An OSR Of 64. The Total Power Consumption Of The Modulator Is 1 MW From A 0.6-V Supply. The Prototype Occupies 2.9 Mm² Using A 0.35- μ m CMOS Technology. Index Terms—Del Apr 1th, 2024

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B. Quadrature Clock Generator The PLL Provides Two 1-GHz 50% Duty-cycle Clocks,clk And Clkq In Fig. 1, That Are Phase Shifted With Respect To One An-other By 90°. As Noted In The Introduction, Quadrature Clocks Simplify The Generation Of The Local 2-GHz Clocks That Are Re-quired In Sections Of The SOC That Are Double-pumped In Order Feb 3th, 2024

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A Compact Switched-Capacitor Regulated Charge Pump Power Supply B. Robert Gregoire, Member, IEEE Abstract—A CMOS Switched-capacitor Reference Is

Combined With A Switched-capacitor Voltage Doubling Charge Pump To Produce A Compact Regulated 3.2-V Power Supply From An Input That Ranges From 1.8 To 3.5 V. It Can Supply Up To 6 MA At Minimum Input.
May 2th, 2024

1186 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. ...

1188 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 6, JUNE 2010 Fig. 4. Comparison Between (a) A Conventional Current-Switch FFE And (b) A Charge-Injection FFE When Data Pattern Is '011'. Fig. 5. Simulated (a) Current, (b) Voltage, And (c) Current In Fig. 1 When An Isolat Jul 1th, 2024

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YI Et Al.: BLE RX FRONT END WITH 1.33-nW SLEEP POWER FOR ENERGY-HARVESTING APPLICATIONS IN

28-nm CMOS 1619 Alternatively, The Sub-0.5-V Energy-harvesting Sources Favor The Use Of An Ultra-low-voltage (ULV) Supply To Build An ULP Radio. In [7], The Supply Voltage (VDD) Is Minimized To 0. May 3th, 2024

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Constraint Is Given By (2) Where, As In (1), Denotes The Time, After The Clock Edge, That And Need To Create A Reasonable Swing At .1 An Interesting Observation In The Above Architecture Is That And (and And) Can Be Merged Because They Evaluate concurrently.2 In other words, the flip flo Apr 3th, 2024

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Source Of Energy, And Unlike Solar Power, It Can Be Harnessed Irrespective Of Illumination Conditions. As Such, Body Heat Is An Ideal Energy Source For Self-powered Wearable Devices [1]. Thermal Energy Can Be Converted To Electrical Energy Using Thermoelectric Generators (TEG), The Solid- Apr 3th, 2024

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Hybrid ...

Bonding And Use This Technology To Create A Multiphase, 40-MHz Buck Converter Supporting A 20-V Input Supply. Our Au-Au Interconnects Between The GaN Chiplet And The CMOS Substrate Are 30 μm In Diameter, And The Die-to-die Standoff Distance Is 50 μm , Resulting In An Interconnect Inductanc Apr 2th, 2024

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IEEE JOURNAL OF SOLID-STATE CIRCUITS 1 In-Memory Computation Of A Machine-Learning Classifier In A Standard 6T SRAM Array Jintao Zhang, Student Member, IEEE, Zhuo Wang, Member, IEEE, And Naveen Verma Member, IEEE, Abstract—This Paper Presents A Machine-learning Classifier Where Computat Jul 3th, 2024

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